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Integration of InGaAs Channel n-MOS Devices on 200mm Si Wafers Using the Aspect-Ratio-Trapping Technique

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We report on the fabrication on InGaAs/InP implant free quantum well (IFQW) n-MOSFET devices on 200mm wafers in a Si CMOS processing environment. The starting virtual InP substrates were prepared by means of the aspect-ratio-trapping technique. Post CMP these substrate resulted in a planar substrate with a rms roughness of 0.32 nm. After channel and gate processing source drain regions were formed by the selective epitaxial growth of Si doped InGaAs. Contact to the source/drain regions was made by a standard W-plug/metal 1 process. The contact resistance was estimated to be on the order of $7 \times 10^{-7} \Omega \cdot \text{cm}^2$. Fully processed devices clearly showed gate modulation albeit on top of high levels of source to drain leakage. The source of this leakage was determined to be the result of the unintentional background doping of the InP buffer layer. Simulations show that the inclusion of the p-InAlAs between the InP and InGaAs can effectively suppress this leakage. This development is a significant step towards the integration of InGaAs based devices on a standard CMOS platform.

Introduction

As CMOS continues to scales to more advanced technological nodes, new higher mobility channel materials will have to be introduced as an alternative to Si in order to meet power and performance requirements [1]. III-V materials and Ge have emerged as an attractive option for nMOS and pMOS respectively. Aside from the difficulties of integrating these new materials in a CMOS flow a critical requirement for their introduction at the ULSI level is that they can be integrated on large size Si wafers. This is a considerable technological challenge as the lattice mismatch between Ge, $\text{In}_{0.53}\text{Ga}_{0.48}\text{As}$ and Si is 4% and 8% respectively. $\text{In}_{0.53}\text{Ga}_{0.48}\text{As}$ devices have been fabricated on 200mm Si wafers by means of growing a thick InAlAs strain relaxed buffer (SRB) layer by MBE [2] but this method is limited by the slow-throughput MBE process and the complexity of ultimately integrating Ge devices on such a pseudo blanket InGaAs wafer. Another approach is to use direct wafer bonding (DWB) to bond a III-V layer to a Ge [3] or Ge-on-Si wafer but this will require 300mm or 450mm donor III-V wafers thereby increasing the cost of the starting material significantly. In contrast, the aspect-ratio-trapping (ART) [4] technique offers an elegant and cost effective solution to

integrating Ge and III-V materials on the same Si wafer. Starting with an STI template, the Si can be recessed and Ge and III-V alternately grown. It has previously been shown that high performance Ge devices can be fabricated from such an STI template [5]. For III-V materials the use of narrow width trenches allows for defects, which result from the lattice mismatch, to be trapped at the STI sidewall. In this work we present the first integration and electrical results of InGaAs devices fabricated on 200mm wafers using the aspect-ratio-trapping technique.

Transistor Process Flow

The main purpose of this work is to investigate the integration of III-V devices in a Si processing environment using virtual substrates generated by the ART process. To this purpose, the test vehicle chosen was that of a planar InGaAs/InP quantum well device. The integration modules developed can be easily ported to a subsequent finfet flow. A schematic of the process flow used to fabricate the InGaAs channel transistors is shown in Fig 1. The flow begins with defining a template for the InP growth in STI wafers. The height of the STI trenches is 300 nm and the width of the active regions is restricted to 100 nm to 200 nm. This gives aspect ratios from 1.5 to 3 which are necessary for the ART process. After the STI process the Si in the active regions is etched in-situ by HCl vapour and a Ge seed layer deposited on which the nominally undoped InP buffer layer is subsequently grown. The InP is overgrown to a level of 300 nm above the level of the STI trenches and the surface then planarized with a CMP step. Post the InP CMP a 15nm InGaAs channel layer is grown. The gate stack is then deposited which comprises of 10 nm Al₂O₃ as the gate dielectric, 10 nm TiN as the gate metal and 80nm SiO which acts as a hardmask. This gatestack is then patterned. The oxide and TiN are dry-etched and the Al₂O₃ is removed by a wetetch. Narrow SiN only spacers are then formed and Si doped InGaAs is selectively deposited to form the source/drain regions. The oxide hardmask is removed from gate pads so that contact can be made to the TiN gate metal. Next the pre metal dielectric (PMD) stack is deposited and planarized. Contacts holes are opened over the InGaAs S/D regions and gate pad. A Ti/TiN liner layer is deposited followed by W which is also planarized. The processing is then completed by using a standard one level Cu metal damascene backend.

Integration Module Development

InP Epitaxy

Starting with the STI template the Si in the active regions is etched in-situ in an CVD reactor by means of a HCl vapour etch thus creating trenches for the subsequent InP growth. Immediately after the Si etch out a thin 50nm Ge seed layer is grown in-situ in the trenches. The Ge layer acts an intermediate buffer layer between the Si and InP. The formation of double steps which can suppress the formation of anti phase boundary (APB) defects can also be more easily promoted on a Ge rather than Si surface [6]. After the thin Ge seed layer growth, the selective area growth (SAG) of the nominally undoped InP buffer layer is carried out using an Aixtron close-coupled showerhead metal-organic vapor phase epitaxy (MOVPE) systems. Trimethylindium (TMIn) was used as the group-III precursor. Tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP) were

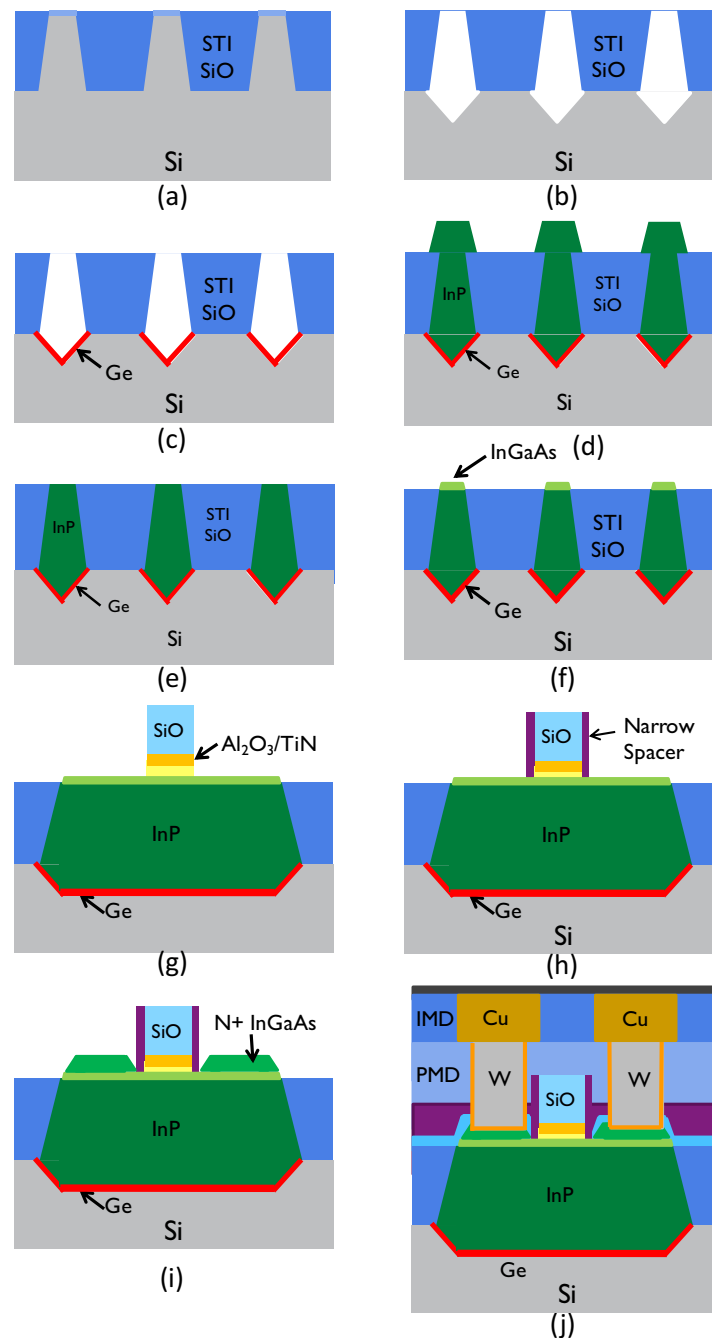


Fig 1: [Color online] Process flow of InGaAs IFQW device. The process starts with an STI template (a). The Si in the trenches is selectively etched (b) and a Ge seed layer deposited (c) on which InP is grown (d). The InP is CMP'd to form a planar surface (e) and the InGaAs channel grown (f). The gate stack is deposited and etched (g) and narrow spacers formed (h). InGaAs N+ S/D regions are grown and the process completed with standard W-plug Metal 1 processing.

employed as the group-V precursors. Before the InP growth, a pre-epi bake at 720 °C and 450 Torr was carried out to remove the Ge native oxide and to promote the formation of double steps. TBAs was introduced during the pre-epi bake to form an As terminated Ge surface that facilitates the InP nucleation [7]. After this thermal treatment the Ge layer is fully relaxed, as confirmed by X-ray diffraction analysis (XRD). Following this bake, the temperature was ramped down to 420 °C for the selective growth of a 30 nm thick InP nucleation or seed layer. Next, the temperature was ramped to 640 °C for the bulk InP SAG. The InP layer was grown to a height of about 300 nm above the level of the STI. More details of the InP growth conditions are described elsewhere [6- 8]. Typical results of the InP growth are shown in Fig. 2. In the direction across the width of the trench the defect density at the top of the trench is low and improves with the aspect ratio of the trench however defects are not fully suppressed in the direction along the length of the trench giving an average defect density on the order of 10^9 cm^{-2} . By using an STI pattern with a more uniform layout of the trenches the defect density can be reduced by an order of magnitude.

InP CMP

The InP overgrowth step is needed as the growth rate of the InP in different width trenches varies because of loading effects. The InP also grows with $\langle 111 \rangle$ facets creating a non-planar surface unsuitable for transistor integration. Therefore a CMP step is needed to planarize the surface before the InGaAs channel deposition [9]. Two different slurries were compared for the CMP process. Slurry A is acidic based and normally used for the CMP of W layers. Slurry B is basic and normally used for the CMP of polysilicon layers. It was found that the acidic based slurry gave better process results (Fig. 3). A cross section of a trench planarized using the acidic slurry is shown in Fig. 4(a). The recess between the InP and the STI SiO layer was measured by AFM to be about 8nm (Fig. 4(b)). AFM analysis of the trenches shows the surface roughness of the InP layer post CMP to be 0.32 nm (rms) (Fig.4 (c)).

InGaAs Channel Growth

Following the CMP of the InP surface the InGaAs channel layer is selectively deposited again using the Aixtron-CRIUS MOCVD reactor. For the InGaAs layer growth we used trimethylindium (TMIn) and trimethylgallium (TMGa) as group-III elements precursors and tertiarybutylarsine (TBAs) for group-V element. Any native oxide formed on the InP layer is first desorbed by means a bake carried out at 500 °C. The InGaAs layer was grown at 520 °C by flowing 16 $\mu\text{mol/min}$ of TMGa, 19 $\mu\text{mol/min}$ of TMIn and 2600 $\mu\text{mol/min}$ of TBAs; the ramping up of the sample temperature was performed under TBP flow (2000 $\mu\text{mol/min}$) and the TBP to TBAs switch was done a number of seconds before allowing the group III precursors in the reactor. The InGaAs layer is nominally undoped.

Cross sectional TEM along the $[-110]$ direction perpendicular to the trenches (Fig. 5(a)) shows a smooth, 15 nm thick InGaAs channel with a sharp InP (001)/InGaAs interface, characterized by a certain degree of roughness that nevertheless seems not to affect the quality of the channel, which exhibits a relatively low density of defects along this direction. $\{111\}$ and $\{113\}$ facets are present at the edges of the InGaAs layer. A SEM tilted image of the grown layer is shown in Fig. 5(c): the InGaAs channel appears smooth but a number of ‘chops’ are visible in the layer. Bright field cross sectional TEM of the III-V layer stack along the $[110]$ direction parallel to the trenches indicates the origin of

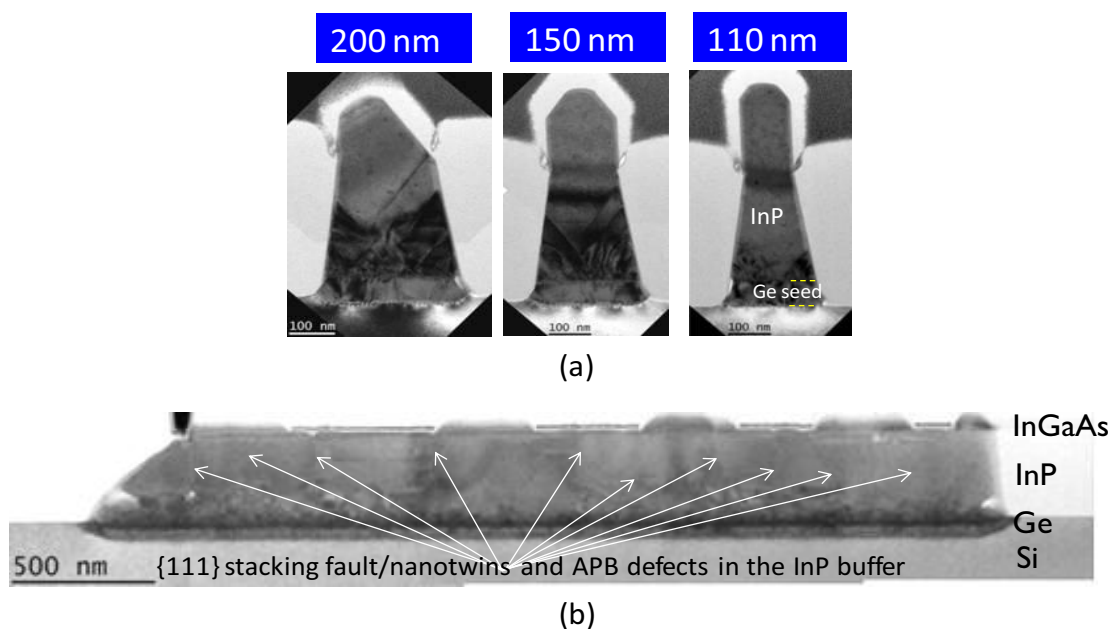


Fig 2: a) Bright field cross-sectional TEM images of different width trenches shows that the quality of the InP increases as the aspect ratio increases b) cross-sectional TEM image along the trench reveals a defect density on the order of 10^9 cm^{-2}

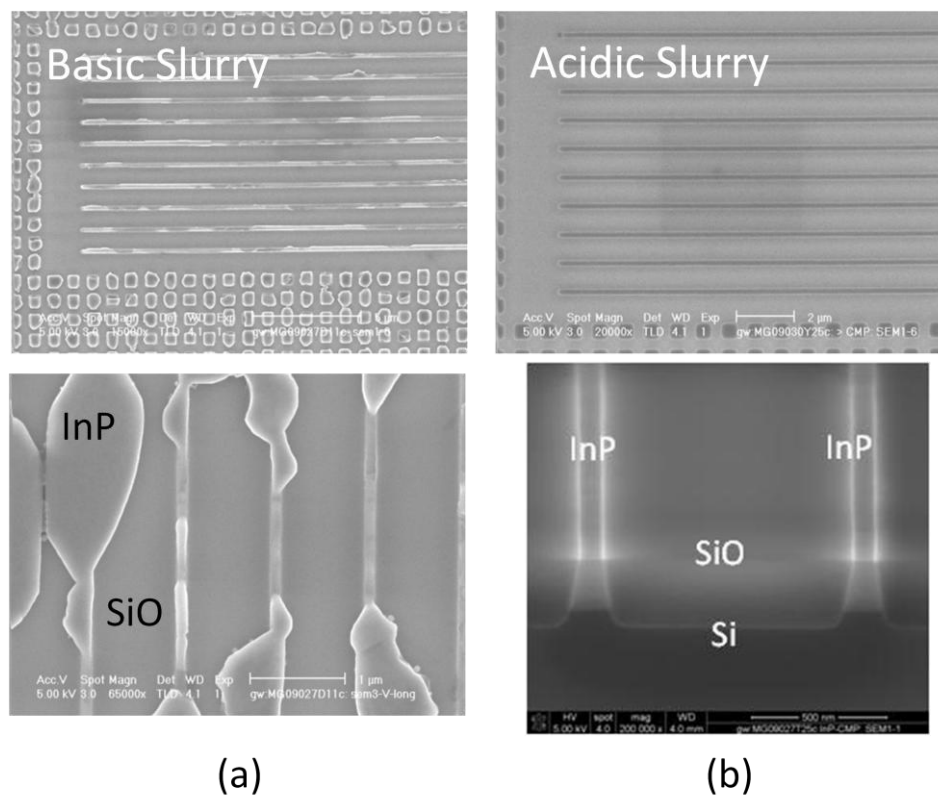


Fig 3: a) Top view SEM images of InP in STI trenches post CMP with basic slurry and b) top view and cross sectional images of the InP post CMP with acidic slurry.

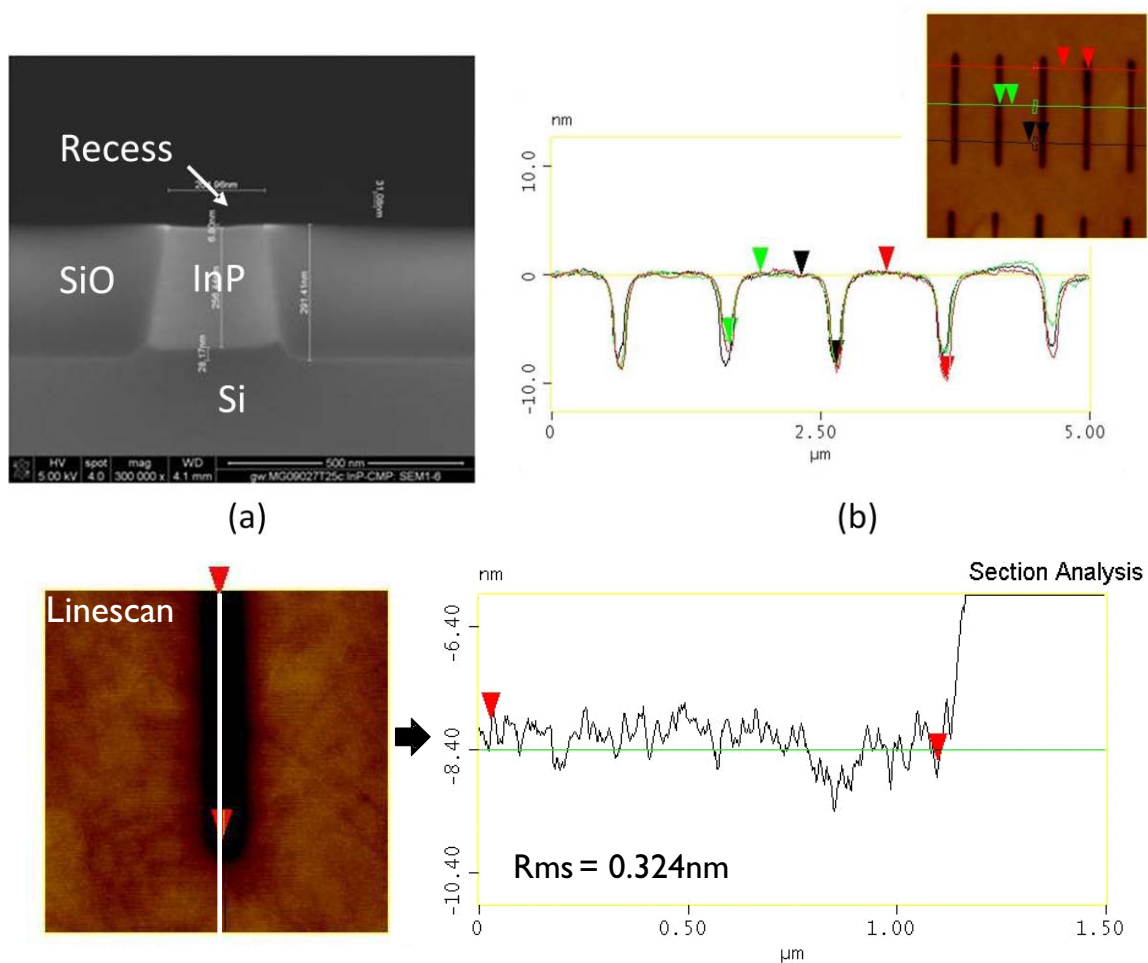


Fig 4: a) [Color online] Cross-sectional XSEM of CMP'd InP. b) The depth of the InP recess inside the STI trench was measured by AFM to be 8nm (c) AFM analysis of the CMP'd InP in the STI trench

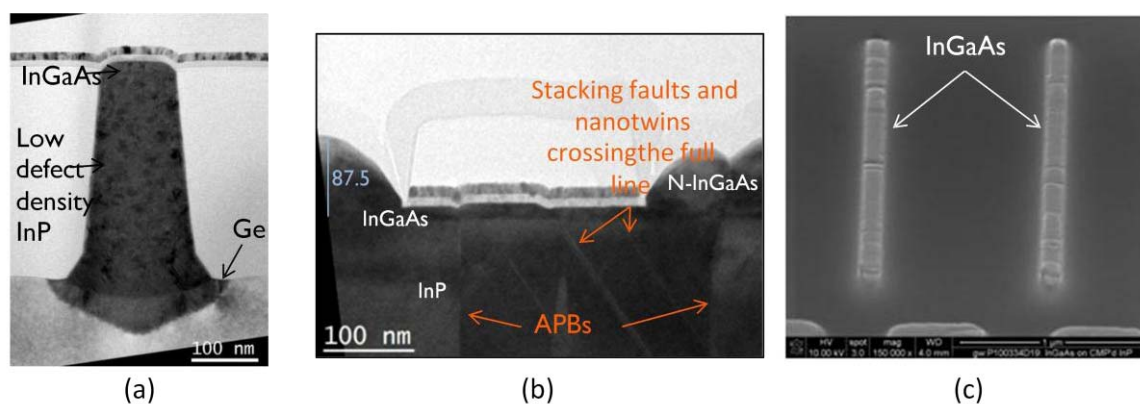


Fig 5: (a) TEM of InGaAs channel growth on the CMP'd InP shows crystalline layer is achieved. (b) Along the length of the trench it can be seen that defects from the InP buffer layer propagate through the InGaAs layer. (c) Top-down SEM view of the InGaAs layer shows 'chops' across the width of the trench which are due to defects in the InP layer as seen in (b).

these features (Fig. 5(b)): grooves form whenever a $\{111\}$ oriented defect (nanotwin, twin, stacking fault) or a $\{110\}$ APB originating at the InP/Ge interface cross the InP/InGaAs interface and reach the surface. Therefore, further defect reduction in the InP buffer layer is needed before improvement in the morphology of the InGaAs channel can be realized.

Gate Stack

For the passivation of InGaAs surfaces we have previously shown that the use of sulfur is effective in creating an unpinned surface with Dit levels on the order of $10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ [10]. However, for these integrated n-MOS devices, the sulfur pre-treatment could not be applied as the aqueous $(\text{NH}_4)_2\text{S}_2$ solution used has a too high metallic contamination level to be used in a VLSI fabrication line. Instead a dilute HCl clean was applied immediately before the high- κ deposition of 10 nm Al_2O_3 by ALD. To apply sulfur treatment in the future an integrated gaseous S vapour solution will be needed [11]. A TEM of the resultant InGaAs/ Al_2O_3 interface is shown in Fig. 6. Some $\{111\}$ defects can be seen in the InGaAs layer but the Al_2O_3 /InGaAs interface is reasonably smooth. The gate stack patterned by the dry etch of the oxide hard mask and TiN gate metal layer. The dry etch stops on the Al_2O_3 which is then removed by wet etch in a 0.03M HF/10% HCl mixture which is selective to InGaAs.

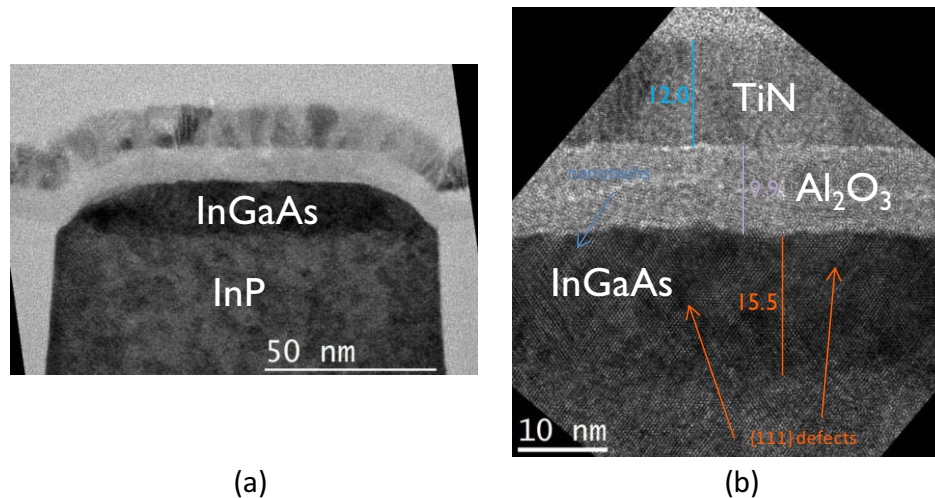


Fig 6: TEM of InGaAs/ Al_2O_3 interface (a). Some $\{111\}$ defects can be seen in the InGaAs layer (b) but the Al_2O_3 /InGaAs interface is reasonably smooth.

N+ InGaAs Source/Drain Processing

After gate patterning, spacers are deposited. For the IFQW architecture a narrow spacer $<10 \text{ nm}$ is required to prevent an excessive access resistance [12,13]. A SiN only spacer process was developed to achieve such a thin layer. After spacer formation the wafers are cleaned in a 0.03M HF/10% HCl solution to help remove any residues or damage from the etch. N+ Si doped InGaAs is then selectively grown to form the source/drain regions. The doping of the InGaAs was estimated from TLM measurements to be on the order of mid to high 10^{18} cm^{-3} levels. TEM analysis of the transistor show that the final spacer thickness

achieved was 6nm (Fig. 7). The InGaAs S/D growth was selective to the SiN and showed no encroachment under the gate.

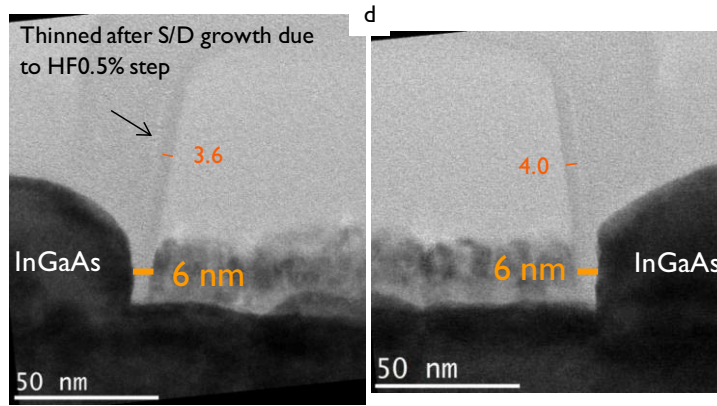


Fig 7: TEM of SiN spacer shows that a 6nm width was achieved. No encroachment of the N+ InGaAs layer underneath the spacer was observed.

Contacts

To form contacts to the InGaAs S/Ds a standard CMOS W-plug scheme was employed. First a PMD stack is deposited and planarized by CMP. Next contact holes are etched. The contacts in this case were drawn as 250 nm x 2 μ m. The large contacts were used to minimize any impact of contact resistance on transistor characteristics. After processing the contact size at the bottom of the hole was about 50nm (Fig 8(a)). The contact etch was not selective to the InGaAs even though a CF₄ based chemistry was used which should in principle be selective to InGaAs so it is possible that physical etching of the layer is taking place. The etch was timed to stop in the InGaAs layer. A 20 nm Ti/10 nm TiN liner layer was then deposited. Before the Ti deposition an in-situ soft sputter Ar etch was used to remove any native oxide. The contact holes were then filled with W followed by a planarization step. The devices are then completed by using a standard one level Cu metal damascene backend. The highest temperature process in this backend is 400 °C.

Physical analysis of the contact by EELS and EDS show that there is no intermixing of the InGaAs and Ti liner layer (Fig. 8(b)). This is an important result as it shows that the non-alloyed ohmic between the InGaAs and Ti can withstand the thermal budget of a standard VLSI CMOS backend. However, the analysis did show that there is still an interfacial oxide between the Ti and InGaAs indicating that the Ar soft sputter etch could be further optimized.

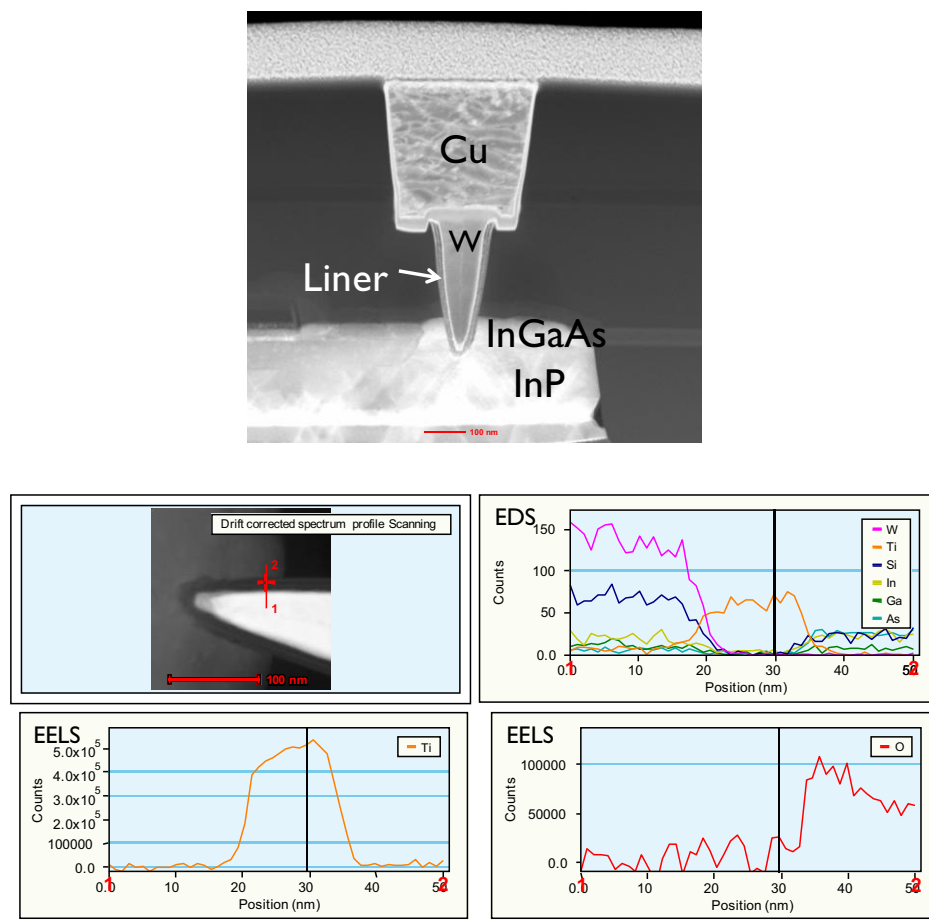


Fig 8: [Color online] TEM of the W-plug contact to the N+ InGaAs S/D layer. The contact etch was not selective to the InGaAs layer. The liner layer consists of Ti/TiN. The width of the contact in the InGaAs layer is about 50 nm. (b) Physical analysis of the contact/InGaAs. EELS and EDS show that there is no intermixing of the Ti from the liner layer and the InGaAs demonstrating that the thermal budget of the backend is low enough. However, oxygen was found at the Ti/InGaAs interface.

Device Results and Discussion

Id-Vgs characteristics

Transistors were fabricated with the process flow described above with the simple InGaAs/InP IFQW architecture. Id-Vgs characteristics of a 130 nm gate length device are shown in Fig. 9. The transistor clearly shows gate modulation but on top of very high levels of source to drain leakage. Physical analysis of the InP grown in the STI implies suggests that this source to drain leakage is a result of the InP layer being conductive. Photoluminescence (PL) measurements of the selectively grown InP are compared to that of a reference InP layer grown on a bulk 2" wafer show a shift in the peak of the response (Fig. 10(a)). This shift corresponds to a n-type doping level on the order of $\sim 10^{17} \text{ cm}^{-3}$. The conductive nature of the InP buffer layer has also been confirmed by 2D scanning spreading resistance microscopy (SSRM) analysis on a fully processed wafer (Fig. 10(b)). The SSRM analysis also showed that the Ge seed layer and underlying Si are also highly

conductive. This has been shown by SIMS measurement to be a result of Phosphorous doping. The thermal budget of the InP buffer layer growth is 640 °C which makes this level of P diffusion quite surprising. The physical mechanism behind the P diffusion into the Ge and Si is under investigation. The source of the n-type doping in the InP is believed to be background C incorporation from the metal organic precursors into the layer during growth.

For the final device structure including an InAlAs layer between the InP and the InGaAs channel is preferred as the conduction band offset between InAlAs/InGaAs (~ 0.5 eV) is higher than that between InP/InGaAs (~ 0.2 eV) [14]. Simulations of this structure show that if the InAlAs is doped p-type and is thick enough the source to drain leakage can be effectively suppressed (Fig. 11). The transport models in the simulations are not calibrated but the results demonstrate the beneficial effects of the p-InAlAs layer on the leakage current.

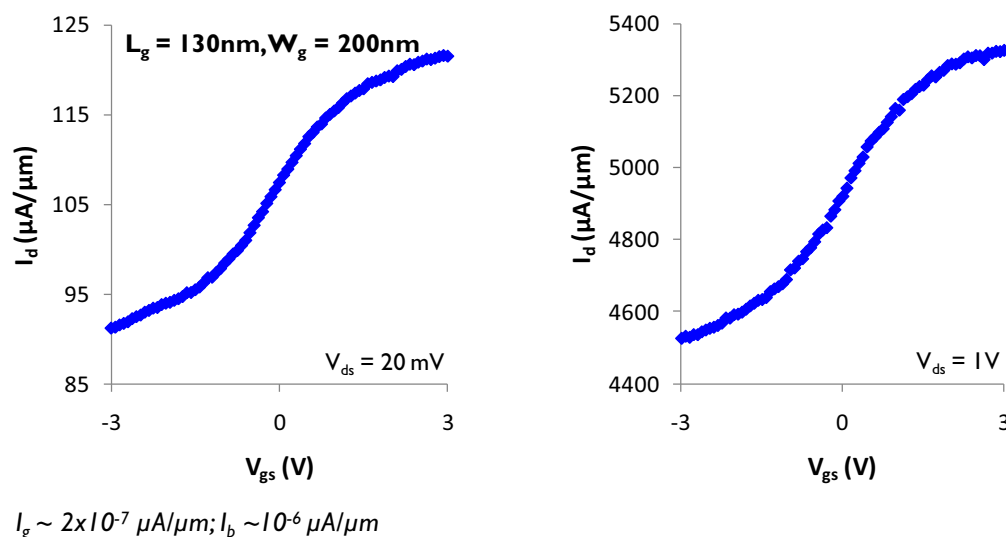


Fig 9: I_d - V_{gs} characteristics of fabricated transistors show gate modulation on top of very high levels of source-drain leakage

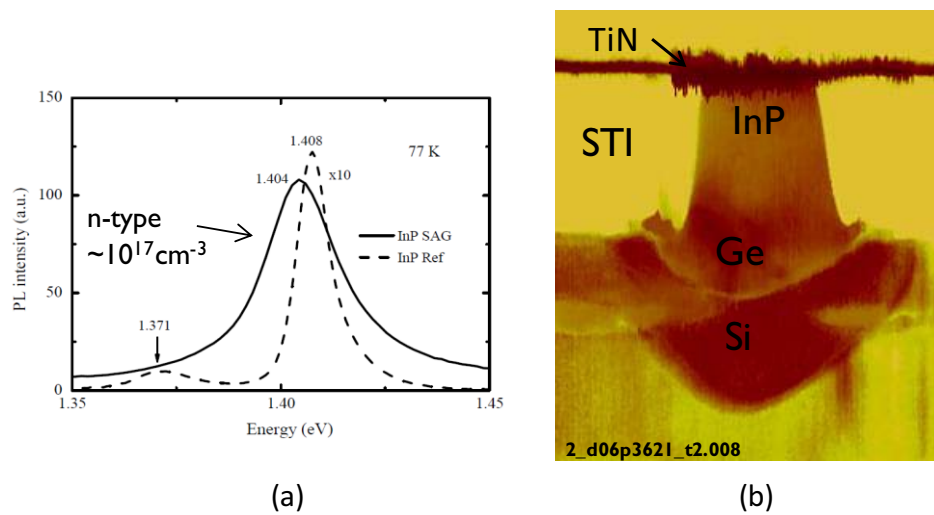


Fig. 10: [Color online] (a) PL measurements of InP grown in STI trenches shows a shift in the peak of the response compared to a blanket InP layer implying a n-type on the order of 10^{17} cm^{-3} . (b) The conductive nature of the InP layer in the trenches is confirmed by SSRM measurements. It is also noted that the Ge and Si regions under the trench are also highly conductive. This has been confirmed by SIMS to be P doped.

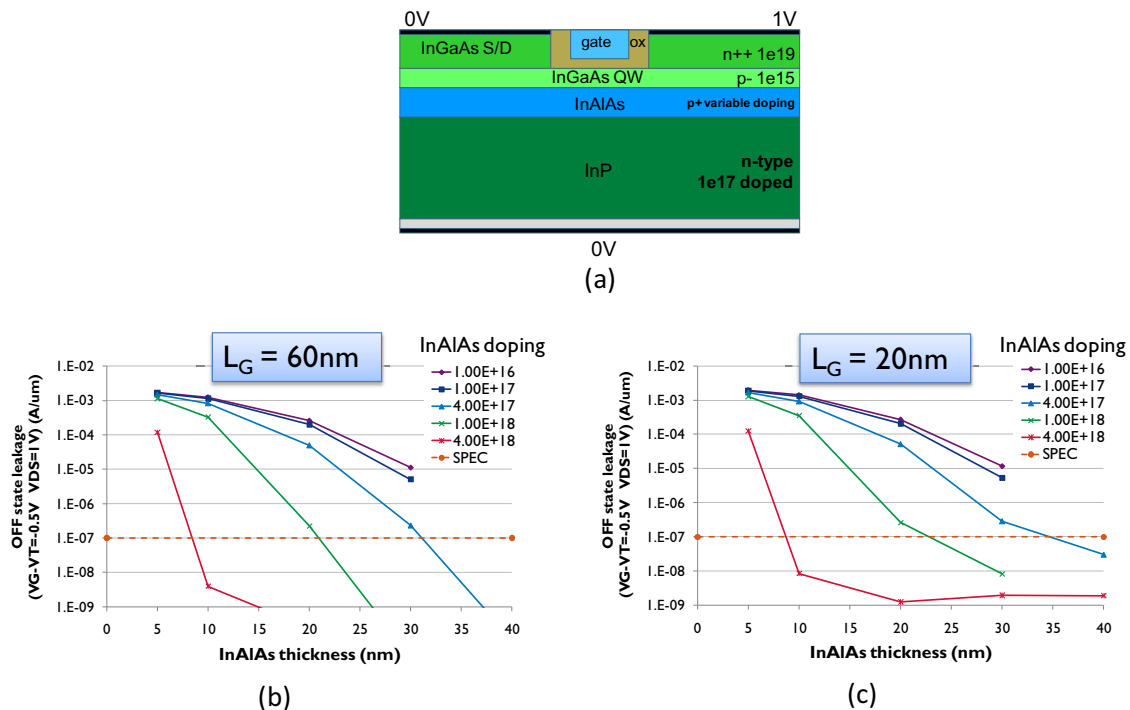


Fig 11: (a) [Color online] Schematic of the structure used to simulate the effect of including a p-type InAlAs layer in the quantum well structure. (b) and (c) Off state leakage for 60 nm and 20 nm gate length devices as a function of the InAlAs layer thickness and doping.

Contact Resistance

TLM measurements of the N+ InGaAs layer yielded an estimate of the specific contact resistivity on the order of $7 \times 10^{-7} \Omega \cdot \text{cm}^2$ (Fig. 12). This is a worse case estimate as we take the whole area of the contact into account. The ITRS roadmap indicates that contact resistances on the order of $5 \times 10^{-8} \Omega \cdot \text{cm}^2$ are required for advanced nodes [15]. In order to achieve a lower contact resistance the InGaAs doping can be increased [16] and/or an InAs contact layer can be used [17].

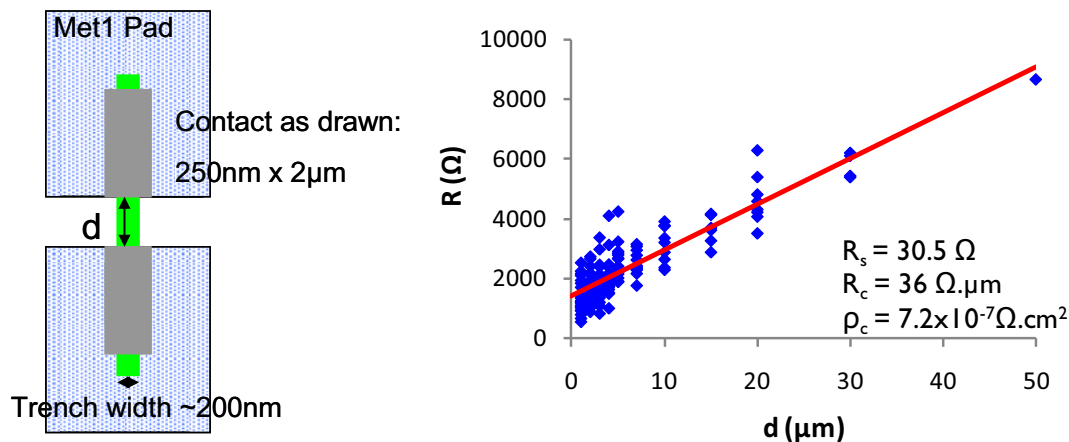


Fig 12: Taking a contact area of $50 \text{ nm} \times 2 \mu\text{m}$, an ρ_c of $7.2 \times 10^{-7} \Omega \cdot \text{cm}^2$ was extracted from TLM measurements.

Conclusions

We have demonstrated the first fully integrated InGaAs n-MOSFET devices processed using the ART technique. The required integration modules to fabricate an InGaAs channel IFQW device were developed in a 200mm Si CMOS processing line. Planar patterned virtual III-V substrates were generated by the growth of an InP buffer layer in a standard Si STI template. The InP layer was subsequently polished giving a rms roughness of 0.32nm. Despite the ART effect along the width of the trench defects still remained in the direction along the length of the trench giving a typical defect density on the order of 10^9 cm^{-2} . These defects are a limiting factor on the morphology of the InGaAs channel layer. Pits in the surface of the channel are observed where dislocations, stacking faults or APB defects reach the surface of the buffer layer. Further optimization of the Ge seed layer and InP buffer growth is required to reduce the level of defects in the channel region. An effective narrow 6nm SiN spacer process was developed for the selective epitaxial growth of Si doped InGaAs source and drain regions. Contact to the N+ source drain regions was achieved through the use of a standard CMOS W-plug process. A worst case contact resistance of $7 \times 10^{-7} \Omega \cdot \text{cm}^2$ was extracted from TLM test structures. Physical characterization of the contacts shows that there is no intermixing of the InGaAs and Ti liner of the W-plug due to the thermal budget of the Metal 1 module ($\leq 400^\circ \text{C}$). The doping of the N+ source drain regions was estimated to be mid to high

10^{18} cm^{-3} levels. Further improvement in the R_c can be achieved by increasing this doping level and adding an InAs capping layer. Fully processed devices showed gate modulation on top of very high levels of source/drain leakage ($\sim \text{mA}/\mu\text{m}$). This leakage was confirmed to be the result of the InP buffer layer being conductive. Simulations show that the leakage can be suppressed by the inclusion of a p-InAlAs layer between the InP and InGaAs channel layer.

While these results demonstrate that many challenges still remain for the integrated of high performance InGaAs devices on a Si platform, they are a significant step towards the realization of an ART based solution.

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References

1. A. Khakifirooz and D.A. Antoniadis, *Trans. Electron. Devices*, **55**, p1401-8, Jun 2008
2. R. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W. Loh, J. Oh, C. Smith, P. Kirsch, P. Majhl and R. Jammy, *IEDM Tech. Digest*, 2010
3. M. Yokoyama, S. Kim, R. Zhang, N. Taoka, Y. Urabe, T. Maeda, H. Takagi, T. Yasuda, H. Yamada, O. Ichikawa, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka and S. Takagi, *VLSI Tech. Digest* 2011
4. E.A. Fitzgerald and N. Chand, *Electron. Mater.*, **20**, pp 839-53, Oct 1991
5. J. Mitard, C. Shea, B. DeJaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W.E. Wang, J. Lin, F. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. DeMeyer, M. Caymax, L. Pantisano, M. Meuris and M. Heyns, *VLSI Tech. Digest*, pp. 82-3, 2009
6. G. Wang, M. Leys, R. Loo, O. Richard, H. Bender, G. Brammertz, N. Waldron. W-E Wang, J. Dekoster, M. Caymax, M. Seefeldt and M. Heyns, *J. Electrochem. Soc.*, **158**(6), H645, 2011
7. G. Wang, M. Leys, N. Nguyen, R. Loo, G. Brammertz, O. Richard, H. Bender, J. Dekoster, M. Meuris, M. Heyns and M. Caymax, *J. Electrochem. Soc.*, **157**(1), H1023 (2010)
8. G. Wang, M. Leys, N. Nguyen, R. Loo, G. Brammertz, O. Richard, H. Bender, J. Dekoster, M. Meuris, M. Heyns and M. Caymax, *J. Cryst. Growth*, **315**, pp 32-6 2011
9. P. Ong, L. Witters, N. Waldron and L. Leunissen, *ECS Trans.* Vol. 34, Issue 1, 2011
10. E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.*, **109**, 024101, 2011

11. A. Alian, G. Brammertz, C. Merckling, A. Firrincieli, W.E. Wang, H.C. Lin, M. Caymax, M. Meuris, K. De Meyer and M. Heyns, *Appl. Phys. Lett.*, **99**,11, pp 112114, Sep 2011
12. G. Hellings, L. Witters, R. Krom, J. Mitard, A. Hikavvy, R. Loo, A. Schulze, G. Eneman, C. Kerner, J. Franco, T. Chiarella, S. Takeoka, J. Tseng, W.E. Wang, W. Vandervorst, P. Absil, S. Biesemans, M. Heyns, K. De Meyer, M. Meuris and T. Hoffmann, *IEDM Tech Digest*, 2010
13. J. Mitard, L. Witters, G. Hellings, R. Krom, J. Franco, G. Eneman, A. Hikavvy, B. Vincent, R. Loo, P. Favia, H. Dekkers, E. Altamirano Sanchez, A. Vanderheyden, D. Vanhaeren, P. Eyben, S. Takeoka, S. Yamaguchi, M. Van Dal, W.E. Wang, S. Hong, W. Vandervorst, K. De Meyer, S. Biesemans, P. Absil, N. Horiguchi and T. Hoffmann, *VLSI Tech. Digest*, 2011
14. M. Radosavljevic, G. Dewey, J.Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. Liu, D.Lubyshev, M.Metz, K. Millard, N. Mukherjee, R. Pan, W. Pillarisetty, W. Rachmady, U. Shah and R. Chau, *IEDM Tech. Digest*, 2010
15. *International Technology Roadmap for Semiconductors*, 2011 Edition
16. A.D. Carter, J. Law, E. Lobisser, G. Burek, W. Mitchell, B. Thibeault, A. Gossard and M. Rodwell, *DRC Conference Proceedings*, pp. 19-20, 2011
17. A. Baraskar, V. Jain, M.A. Wistey, U. Singiseti, Y.U. Lee, B. Thibeault, A. Gossard and M. Rodwell, *IPRM Conference Proceedings*, July 2010